

Pulse-Width Modulation (PWM)

Modules: Integrate & Dump, Digital Utilities, Wideband True RMS Meter, Tuneable LPF, Audio Oscillator, Multiplier, Utilities, Noise Generator, Speech, Headphones.

0 Pre-Laboratory Reading

Pulse-width modulation (PWM) is a signaling format that is commonly used by microcontrollers for communicating with certain types of peripherals, such as motors. PWM is also used in radio-frequency identification (RFID) systems and in radio-controlled (RC) model airplanes, boats and vehicles.

0.1 Baseband PWM

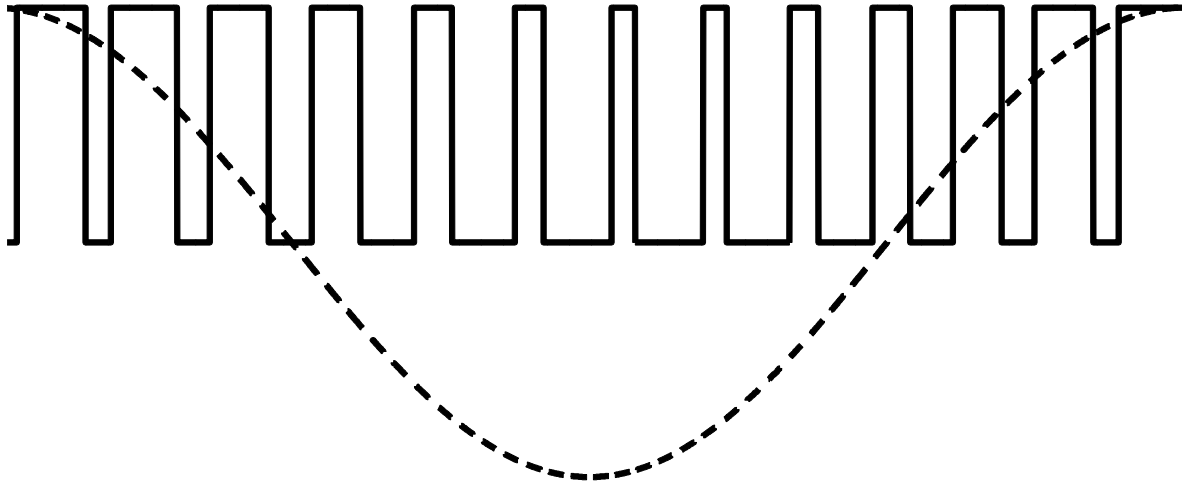
PWM employs a train of pulses. All pulses are flat-topped and have the same amplitude. The pulse repetition rate (that is, the number of pulses per second) is constant. Information is conveyed by the width of the pulses. When an analog signal is sampled, each sample value can be encoded in the width of a pulse. The pulse repetition rate is then equal to the sampling rate.

Most PWM systems are designed so that the width w of an individual pulse is related to the corresponding sample value x by

$$w = a + bx \tag{1}$$

where a and b are constants. The purpose of the (positive) coefficient a is to ensure that the pulse width, which by definition must always be positive, can encode both positive and negative values of x . The coefficient b can be either positive or negative. When b is positive, the pulse width becomes larger as the sample value becomes larger. When b is negative, the pulse width becomes smaller as the sample value becomes larger. In the PWM channel in the Integrate & Dump module, b is negative. However, we can place an amplifier with negative gain between the source of the samples and the PWM channel; and then the coefficient b for the composite system (comprising the amplifier and the PWM channel) is positive.

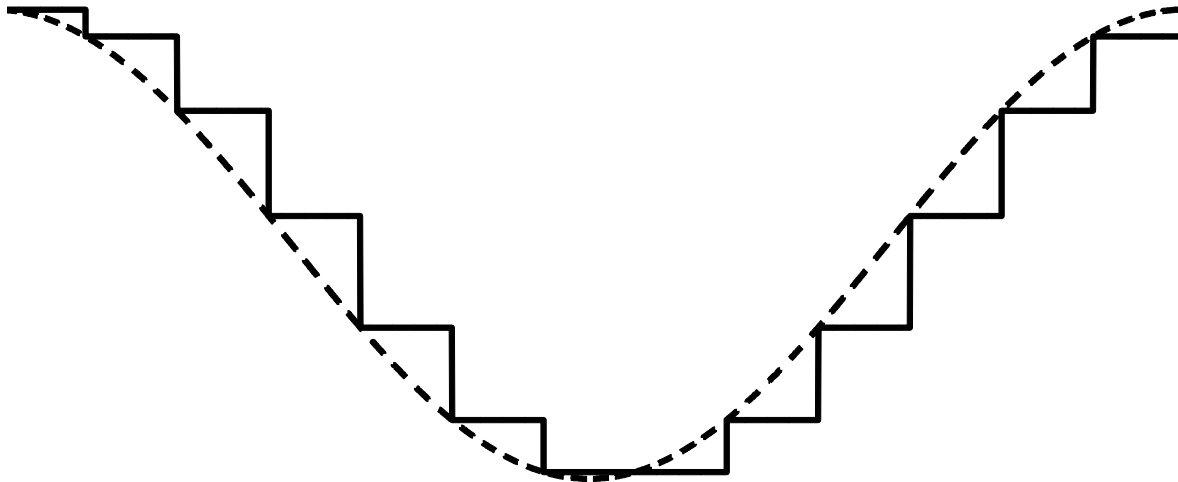
The figure below illustrates baseband PWM. The term “baseband” emphasizes the fact that there is no radio-frequency (RF) carrier in this modulation scheme. In this figure, the dashed curve is the original signal and the solid curve is the PWM signal. The coefficient b is positive in this illustration. The PWM signal is binary valued. Each pulse has the same positive value, and the “spaces” between pulses have the value zero.



Baseband PWM: original signal (dashed) and PWM signal (solid); positive b

In order to demodulate a baseband PWM signal, it is usual first to convert the PWM signal to a pulse-amplitude modulation (PAM) signal. This conversion is done with an integrate-and-hold device. For this to work, it is essential that the integrate-and-hold device be controlled by a clock of the same frequency as that which controls the PWM process. The integration occurs over one pulse repetition period (the reciprocal of the pulse repetition rate), and then the result of this integration is held for one pulse repetition period. Since the amplitude is the same for all pulses in a PWM pulse train, any one integration gives a value that is proportional to the width of the pulse on the input. Hence, the information which lies in the pulse width of the input PWM signal now lies in the amplitude of the output PAM signal.

When the PWM signal illustrated above is sent to an integrate-and-hold device, the result appears below. As you can see, the pulse width is now constant and the information is now encoded in the pulse amplitudes. This PAM signal is a staircase approximation of the original analog signal. (The integrate-and-hold channel in the Integrate & Dump module includes a negative sign; this sign can be canceled by amplification with a negative gain. The figure below assumes that this has been done.)



Baseband PAM signal: original signal (dashed) and PAM signal (solid)

The final step in the demodulation process is to send the PAM signal to a lowpass filter. The filter bandwidth should be larger than the bandwidth of the original signal and smaller than the pulse repetition rate.

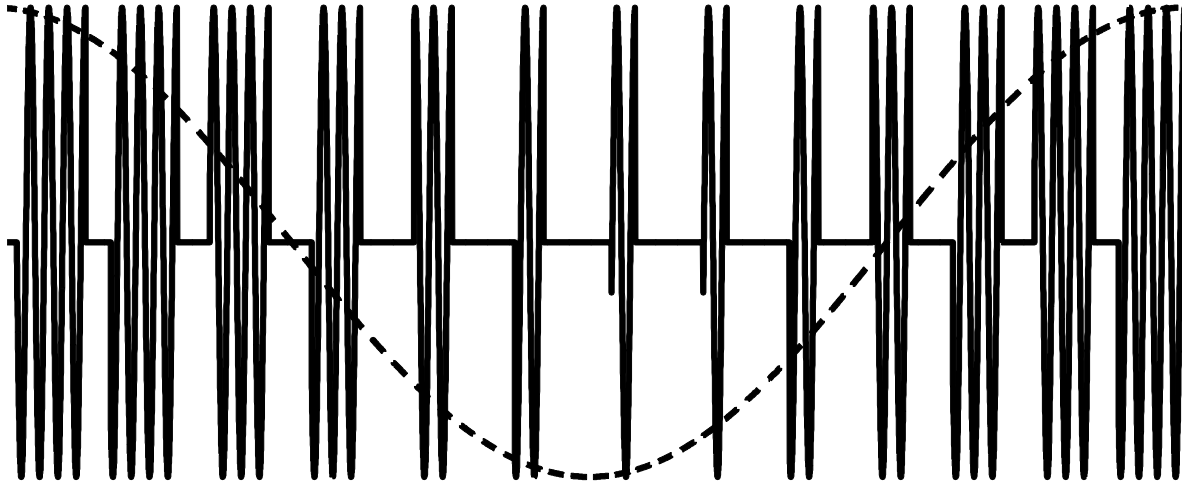
0.2 PWM on an RF carrier

For some applications that employ PWM, an RF carrier is needed because the signal will be propagated wirelessly. RFID and RC systems are examples of this.

A baseband PWM signal can multiply a sinusoidal RF carrier. This creates a carrier that is double-sideband (DSB) modulated with a PWM signal. Therefore, there are really two layers of modulation here.

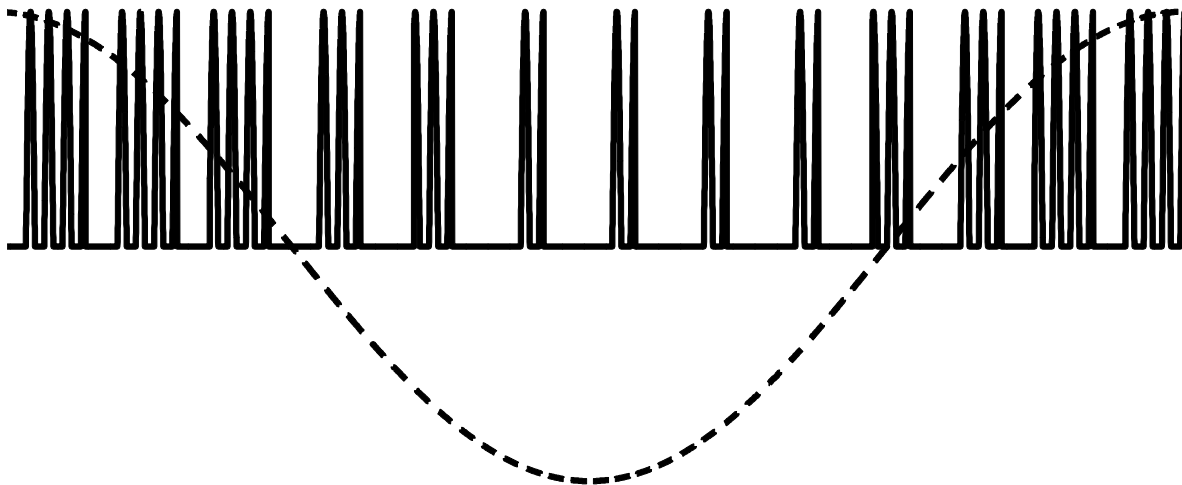
Ordinarily, a DSB carrier is demodulated with a synchronous demodulator. However, in this case, the carrier is only present part of the time. (In between PWM pulses, the carrier is absent.) If the receiver is remote from the transmitter, as will normally be the case once our equipment is removed from the laboratory and placed in operation, there is no carrier that the receiver can steal. Moreover, a phase-locked loop won't work in this application because the carrier is absent much of the time. (A phase-locked loop cannot track a carrier that is constantly disappearing and reappearing.)

Envelope detection finds the envelope of a carrier. In ordinary DSB this is not acceptable because the envelope represents the absolute value of the message, rather than the message itself. However, in the present case, the signal that modulates the carrier is a PWM signal, which is everywhere non-negative. (That is to say, it is always either positive or zero.) So envelope detection can be used for DSB when the modulating signal is a PWM signal.



PWM with an RF carrier: original signal (dashed) and PWM/DSB carrier (solid)

When the PWM/DSB carrier is placed at the input of a rectifier, the output looks like this:

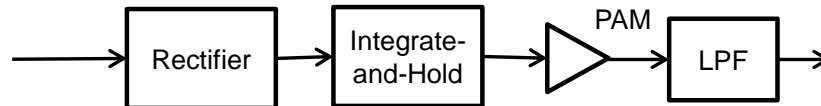


Rectified carrier: original signal (dashed) and rectified PWM/DSB carrier (solid)

In words, the rectifier retains the positive half cycles and nulls the negative half cycles. The demodulation of the carrier can be completed by placing the rectifier output at the input of an integrate-and-hold device such that the period of each integration equals the pulse repetition period. The integrator output corresponding to any given pulse will be proportional to the duration of that pulse. Hence, the output of the integrate-and-hold device is a PAM signal. It

should be noted that the rectifier plays an essential role in this demodulator. If an unrectified PWM/DSB carrier were placed at the input of an integrator, the negative and positive half cycles would cancel out, causing the signal to disappear.

The PAM signal can then be sent to a lowpass filter, and this produces a replica of the original analog message signal. The filter bandwidth should be larger than the bandwidth of the original analog message signal, and the filter bandwidth should be smaller than the pulse repetition rate. The complete demodulator for a PWM/DSB carrier looks like this:



The truth be told, the integrate-and-hold device can be removed from the above arrangement, as long as the bandwidth of the lowpass filter is much less than the pulse repetition rate (but larger than the bandwidth of the message signal). The abbreviated configuration for the demodulator is therefore:



The fact that the integrate-and-hold device is not absolutely necessary for this demodulator can be understood as follows. An integrator is a special type of lowpass filter. Two lowpass filters in series can be replaced with one lowpass filter, assuming the one filter has a suitable bandwidth.

1 PWM with a DC Input Voltage

The Integrate & Dump module can be configured for PWM. Only the first (upper) channel on this module can be so configured. On the PCB, set the rotary switch corresponding to the first channel to PWM mode. Later in this experiment you will be using the second (lower) channel in the integrate-and-hold mode, so you should go ahead and set the second rotary switch accordingly.

Connect the Variable DC output into the first channel of the Integrate & Dump module (set for PWM). Place a TTL signal with frequency equal to $(100/24)$ kHz at the clock input of the Integrate & Dump module. You will create this clock (of approximately 4.17 kHz) by placing the 8.3-kHz TTL (Master Signals) clock, with a frequency of $(100/12)$ kHz, at the input to a divide-by-2 on the Digital Utilities module. Monitor the Variable DC output using the Wideband True RMS Meter. Recall that the root-mean-square of a DC signal is the absolute value of that signal.

Set the PWM input voltage x to zero. Place a copy of the (100/24)-kHz TTL clock on Channel A of the oscilloscope. Connect the PWM output to Channel B. Use the Channel-A signal (the TTL clock) as the trigger source. (The trigger level should be non-zero and positive.)



Channel A: (100/24)-kHz TTL clock

Channel B: PWM output with $x = 0$

You should notice that for an input voltage of zero, the PWM output is a sequence of pulses with a duty cycle of approximately 50%. (That is, the PWM output is high about half the time and low the other half.)

You will now experiment with other (non-zero) values for the input voltage. You should find that when the input voltage is non-zero and positive, the PWM output pulses are narrower than for the case of zero input. That is to say, with a positive input, the duty cycle is less than 50%. As the input voltage increases, the output pulses become narrower. The falling edges of the output pulses are stationary relative to the clock (the Channel-A signal). When the input voltage is increased, each rising edge occurs later, closer to the next falling edge.

For several input voltages between 0 V and +1 V, you are to measure the pulse width and record the data in an Excel worksheet. Use two time rulers on the oscilloscope to measure pulse width.



PWM with DC input voltage

You should find that these data define (approximately) a straight line. The straight line should have the (approximate) mathematical form of Eq. (1), where $a = T_{\text{clk}}/2$ seconds, b is negative (and in units of s/V), and x is the (sample) voltage at the PWM input. T_{clk} is the period (in seconds) of the TTL clock that controls timing for the PWM, and so T_{clk} is the reciprocal of the TTL clock frequency.

Looking at the data of your Excel worksheet, estimate the (negative) slope of this line in units of seconds/volt. Make a note of this slope because you will need it later.



Show your value of b , the negative slope (in s/V), to your instructor.

Now experiment with negative input voltages. (The Variable DC panel produces a negative voltage when its knob is rotated counter-clockwise from the zero-volt position.) You should find that the PWM output pulses are wider than the pulse width in the case of zero input. That is to say, with a negative input, the duty cycle is greater than 50%.

This PWM device is useful only if the input voltage lies within a restricted range. If the input voltage is positive and too large, the output pulses disappear. If the input voltage is negative with an absolute value that is too large, the output pulses coalesce. We cannot convey

information by means of pulse width in either of these two limiting cases. Therefore, it is important to specify the acceptable range of values for the input voltage.

As a practical limit on positive values of the input voltage x , we will say that a positive x should not result in a width w that is smaller than $T_{\text{clk}}/8$. From Eq. (1), with $a = T_{\text{clk}}/2$, this becomes an inequality:

$$w = \left(\frac{T_{\text{clk}}}{2}\right) + bx \geq \frac{T_{\text{clk}}}{8} \quad (2)$$

or, rearranging terms,

$$x \leq \frac{3}{8} \cdot \frac{T_{\text{clk}}}{-b} \quad (3)$$

It should be remembered that b is negative and that, therefore, $-b$ is positive.

We want to generalize the limit of Inequality (3) to cover the case of negative as well as positive values of x . An appropriate constraint on x is:

$$|x| \leq \frac{3}{8} \cdot \frac{T_{\text{clk}}}{|b|} \quad (5)$$

As you can see from this inequality, the maximum permitted value for $|x|$ is inversely proportional to the clock frequency.

For the case of a (100/24)-kHz clock, calculate the maximum permitted value for the input voltage according to Inequality (5). In your experimental set-up, set the input voltage to this (positive) maximum. With the (100/24)-kHz TTL clock on Channel A and the PWM output on Channel B, observe the PWM output.



Channel A: (100/24)-kHz TTL clock

Channel B: PWM output with x set to maximum value permitted by Inequality (5)

For the case of a (100/12)-kHz clock, calculate the maximum permitted value for the input voltage according to Inequality (5). Modify your experimental arrangement so that the 8.3-kHz TTL clock, which has a frequency of (100/12) kHz, goes directly into the clock input of the PWM (thereby by-passing the divide-by-2). Set the input voltage to the maximum permitted value for the (100/12)-kHz clock and observe the PWM output.



Channel A: (100/12)-kHz TTL clock

Channel B: PWM output with x set to maximum value permitted by Inequality (5)



Plot pulse width w as a function of PWM input voltage x (for x between 0 V and +1 V). Use discrete point.

2 PWM with a Sinusoidal Input Voltage

You will now use a sinusoid as the input to the PWM process. Connect the Audio Oscillator to one of the Buffer Amplifiers and the output of this amplifier to the PWM channel of the Integrate & Dump module. Adjust the frequency of the Audio Oscillator to 400 Hz. Place a TTL clock of frequency (100/24) kHz on the clock input of the Integrate & Dump module.

Adjust the absolute value of the amplifier gain so that the sinusoid at the input to the PWM channel has an amplitude equal to the maximum voltage permitted by Inequality (5). (If you are measuring the rms voltage of the PWM input, don't forget that the amplitude of a sinusoid equals $\sqrt{2}$ times the rms voltage.)

Place a copy of the Audio Oscillator output on Channel A, and connect the PWM output to Channel B. Since the frequencies of the signals on Channels A and B are not related, it is not possible to stabilize (freeze) both signals simultaneously without stopping the capture of the signals. Use the TTL output of the Audio Oscillator as the (external) trigger for the scope, so that the 400-Hz sinusoid will be stabilized. (You will probably want to occasionally stop the capture of signals in order to get a static scope display, but this means that you will have to start capturing again whenever anything in the experimental configuration changes.)



Channel A: Audio Oscillator output

Channel B: PWM output

You should notice that the output pulses are wider when the Audio Oscillator output is positive and narrower when the Audio Oscillator output is negative. This behavior results from using a Buffer Amplifier with negative gain, causing the coefficient b for the composite system (including the Buffer Amplifier) to be positive.

3 Pulse-Amplitude Modulation (PAM)

The information contained in the pulse width of a PWM signal can be placed instead in the amplitude of a pulse. The result is pulse-amplitude modulation (PAM). A PWM signal can be converted to a PAM signal with an integrate-and-hold operation. A PWM signal is placed at the input to an integrate-and-hold device, and the same clock used to create the PWM signal is used to control the integrate-and-hold operation. This produces a train of pulses with the following properties. The individual pulse is flat-topped, but the pulse amplitude varies from one pulse to the next. In fact, the amplitude of any given pulse in the PAM signal is proportional to the width of the corresponding pulse in the PWM signal. Hence, both signals convey the same information.

The Audio Oscillator, with a frequency of 400 Hz, should still be connected to a Buffer Amplifier, and this amplifier should still feed the PWM channel. The amplitude of the sinusoid at the PWM input should still equal the maximum voltage permitted by Inequality (5). Place the PWM signal (the output of the first channel) on the input of the integrate-and-hold device (the second channel of the Integrate & Dump module). The (100/24)-kHz clock will control the operation of both the PWM channel and the integrate-and-hold channel. Connect the output of the integrate-and-hold device to the input of the second Buffer Amplifier. (The integrate-and-hold operation introduces a negative sign, and the Buffer Amplifier introduces a second negative sign. Thus, the negative signs cancel.)

Place a copy of the PWM output on Channel A, and connect the output of the second Buffer Amplifier (the amplifier which applies a negative gain to the integrate-and-hold output) to Channel B. Use the TTL output from the Audio Oscillator as an external trigger source. (You can't stabilize all signals at once on the display, so you will want to stop signal capture on occasion.)



Channel A: PWM output

Channel B: PAM output (output from second Buffer Amplifier)

You should observe that the Channel A signal encodes the information in the width of pulses while the Channel B signal encodes the information in pulse amplitudes.

4 Demodulation of PWM

Now you will demodulate the PWM output. This is commonly done in a two-stage process. First, the PWM signal is converted to a PAM signal. Second, the PAM signal is applied to a lowpass filter.

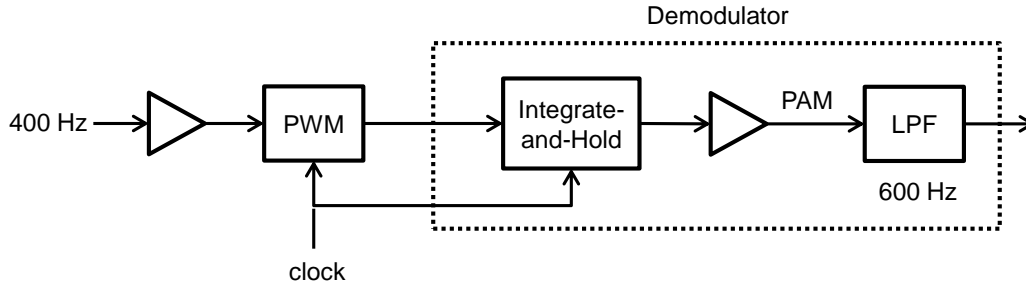
Use the same configuration as in Part 3. The PWM input will be a sinusoid with a frequency of 400 Hz and an amplitude that is the maximum permitted by Inequality (5). A (100/24)-kHz clock will control the timing of both the PWM and integrate-and-hold channels.

You will use a Tuneable LPF in the demodulator. Before placing it in the demodulator, adjust its bandwidth to approximately 600 Hz. (The Tuneable LPF's clock output has a frequency equal to 100 times the bandwidth.) Use the Noise Generator module to get a quick display of $|H(f)|$.



Channel A: Tuneable LPF output, showing $|H(f)|$.

Connect the output of the second Buffer Amplifier (the amplifier that applies a negative gain to the integrate-and-hold output) to the input of the Tuneable LPF. Your configuration should now look as follows. You should note that we regard the integrate-and-hold operation together with the lowpass filtering as a demodulator of a PWM signal.



Connect the output of the Audio Oscillator on Channel A and the output of the demodulator (the output of the 600-Hz LPF) on Channel B. The demodulator output contains a DC component that is unrelated to the signal of interest. Use AC coupling for Channel B, in order to block this DC component.

 Channel A: Audio Oscillator output
 Channel B: demodulator output

The demodulator output (with the DC component removed) should be a reasonable approximation of the original message sinusoid, allowing for scaling and delay.

5 PWM on a Carrier

Remove the demodulator portion of your experimental arrangement from Part 4, leaving just the baseband PWM modulator. The PWM input will be a sinusoid with a frequency of 400 Hz and an amplitude that is the maximum permitted by Inequality (5). The PWM channel should be clocked at $(100/24)$ kHz, as above.

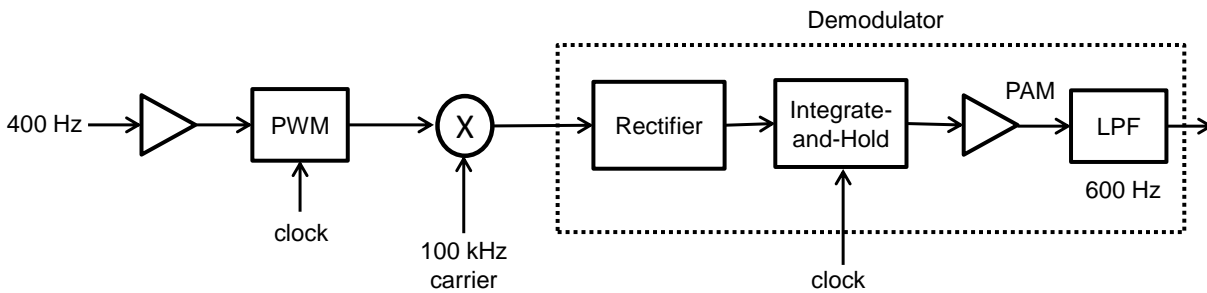
Place the baseband PWM signal at one input of the Multiplier and a 100-kHz carrier on the other input. It is essential that the Multiplier be set for DC coupling. When the PWM output is zero (that is, between pulses) the carrier must also equal zero, and this can only happen with DC coupling. This implements DSB modulation of the 100-kHz carrier. Therefore, both PWM and DSB modulation are present. Place a copy of the Audio Oscillator output on Channel A, and connect the Multiplier output to Channel B. Use the TTL output from the Audio Oscillator as the external trigger.

 Channel A: Audio Oscillator output
 Channel B: Multiplier output

Connect the Multiplier output to the Rectifier (within the Utilities module). Connect the Rectifier output to Channel B, using the Audio Oscillator TTL output as an external trigger.


 Channel A: Audio Oscillator output
 Channel B: rectifier output

Connect the Rectifier output to the input of the integrate-and-hold device. Connect the output of the integrate-and-hold device to the input of the second Buffer Amplifier. The (100/24)-kHz clock will control the operation of both the PWM channel and the integrate-and-hold channel. The output of this second Buffer Amplifier will be a PAM signal. Connect this PAM signal to the Tuneable LPF, adjusted for a bandwidth of 600 Hz. Your configuration should now look like this:



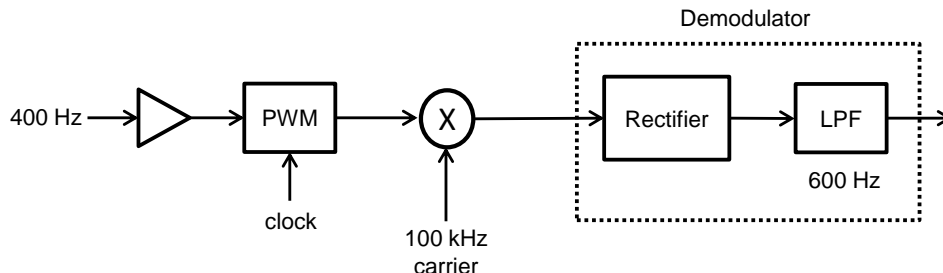
The combination of the rectifier and the integrate-and-hold demodulates the RF carrier and converts PWM to PAM. The LPF recovers the original analog message from the PAM signal.

Place a copy of the Audio Oscillator output on Channel A, and connect the demodulator output (the 600-Hz filter output) to Channel B. Use the Audio Oscillator TTL output as an external trigger. Set Channel B for AC coupling.

-  **Channel A:** Audio Oscillator output
- Channel B:** demodulator output (full DSB/PWM demodulator)

The demodulator output should be a reasonable approximation of the original message sinusoid, allowing for scaling and delay.

Now remove the integrate-and-hold device, along with the following (negative-gain) amplifier. The new configuration should look like this:



You should have a copy of the Audio Oscillator output on Channel A and the 600-Hz LPF output on Channel B. Use the Audio Oscillator TTL output as an external trigger. Make sure that Channel B is set for AC coupling.



Channel A: Audio Oscillator output

Channel B: demodulator output (simplified DSB/PWM demodulator)

You should find that the simplified demodulator output is a reasonable approximation of the original message sinusoid, allowing for scaling and delay.

6 PWM with Speech

Substitute an audio signal from the Speech module for the 400-kHz sinusoid in the configuration of Part 5 (without the integrate-and-hold device). Listen to the recovered signal (coming out of the Tuneable LPF) using the headphones. Try to improve the quality of the recovered signal.

Here are some changes that you can make. Use a larger pulse repetition rate (the frequency of the TTL clock input that controls the PWM channel). It is suggested that you use the 8.3-kHz TTL clock for this purpose. Increase the bandwidth of the lowpass filter in the demodulator. Adjust the gain of the Buffer Amplifier that amplifies the signal that goes into the PWM channel.